DELAY LOCK LOOP USING SHIFT REGISTER WITH TOKEN BIT TO SELECT ADJACENT CLOCK SIGNALS

ABSTRACT

Delay lock loop (DLL) circuits, systems, and methods providing glitch-free output clock signals. Glitches are eliminated from an output clock signal by using shift registers including a single token bit to select one of many delayed clock signals. A DLL clock multiplexer includes a series of shift registers, each of which selects only one of the many input clock signals at each stage. Thus, only one clock signal is selected at any given time. Delay is added or subtracted from the loop by shifting the token bit within each shift register. The token bit is shifted by a single position at a time. Therefore, no glitching occurs.